

# INTEL® PARALLEL STUDIO XE ANALYZERS AND CLUSTER TOOLS OVERVIEW

For Distributed Performance

## Agenda

#### Intel VTune Amplifier

Overview, Predefined Analysis, VTune Platform Profiler, Demo

#### **Intel Advisor**

Vectorization Advisor, Roofline, Demo

#### Intel Inspector

Overview, Demo

#### Intel® MPI Library

Basic Usage, Heterogeneous Jobs, Intel MPI Benchmarks, mpitune

#### Intel® Trace Analyzer and Collector

Overview, Demo



## Faster, Scalable Code, Faster

Intel® VTune™ Amplifier Performance Profiler

#### **Accurate Data - Low Overhead**

CPU, GPU, FPU, threading, bandwidth...

#### Meaningful Analysis

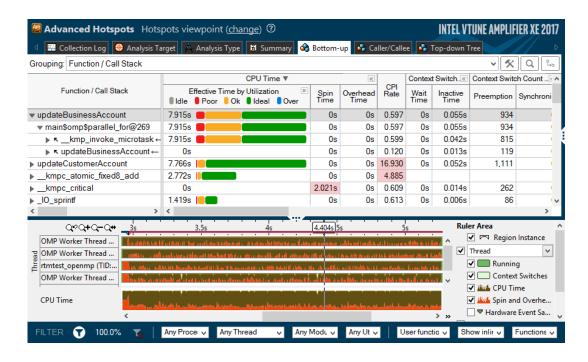
- Threading, OpenMP region efficiency
- Memory access, storage device

#### Easy

- Data displayed on the source code
- Easy set-up, no special compiles

"Last week, Intel® VTune™ Amplifier helped us find almost 3X performance improvement. This week it helped us improve the performance another 3X."

Claire Cates
Principal Developer
SAS Institute Inc.



http://intel.ly/vtune-amplifier-xe

## Two Great Ways to Collect Data

#### Intel<sup>®</sup> VTune<sup>™</sup> Amplifier

Software Collector	Hardware Collector		
Uses OS interrupts	Uses the on chip Performance Monitoring Unit (PMU)		
Collects from a single process tree	Collect system wide or from a single process tree.		
~10ms default resolution	~1ms default resolution (finer granularity - finds small functions)		
Either an Intel® or a compatible processor	Requires a genuine Intel® processor for collection		
Call stacks show calling sequence	Optionally collect call stacks		
Works in virtual environments	Works in a VM only when supported by the VM (e.g., vSphere*, KVM)		
No driver required	Requires a driver - Easy to install on Windows - Linux requires root (or use default perf driver)		

No special recompiles - C, C++, C#, Fortran, Java, Assembly



## Find Answers Fast

Intel<sup>®</sup> VTune<sup>™</sup> Amplifier

#### Adjust Data Grouping

Function - Call Stack

Module - Function - Call Stack

Source File - Function - Call Stack

Thread - Function - Call Stack

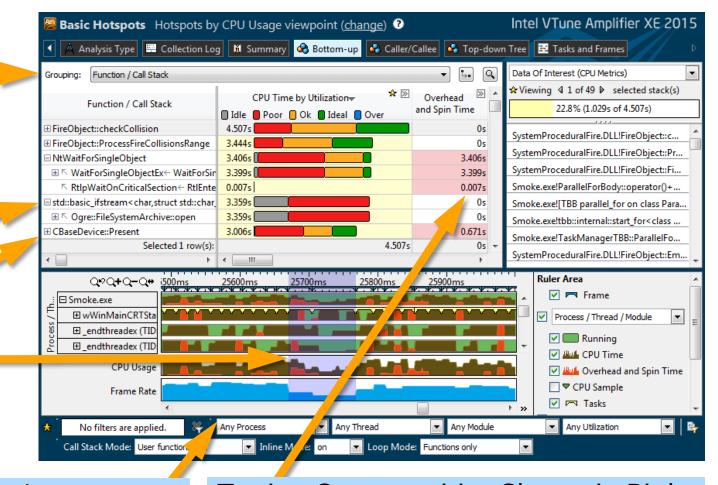
... (Partial list shown)

Double Click Function to View Source

Click [+] for Call Stack

Filter by Timeline Selection (or by Grid Selection)

Zoom In And Filter On Selection
Filter In by Selection
Remove All Filters



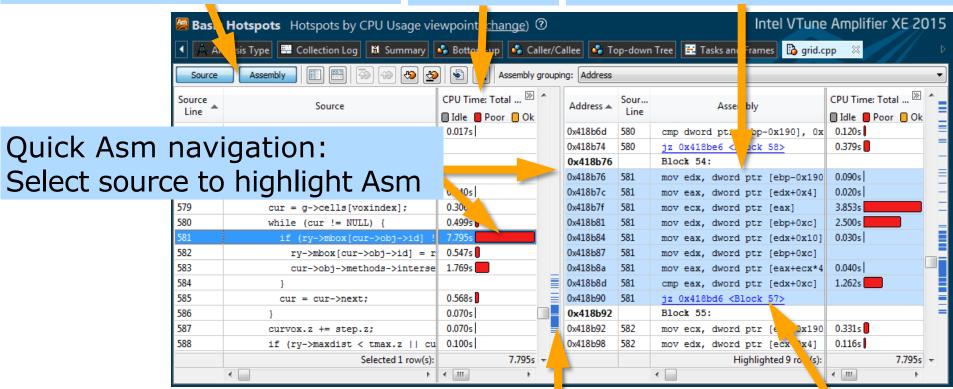
Filter by Process & Other Controls

Tuning Opportunities Shown in Pink. Hover for Tips

## See Profile Data On Source / Asm

Double Click from Grid or Timeline

View Source / Asm or both CPU Time Right click for instruction reference manual



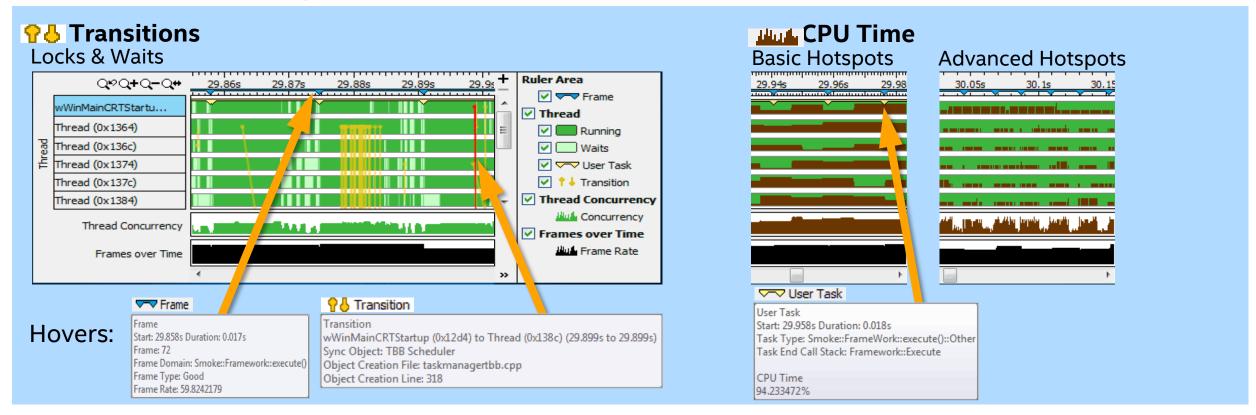
Scroll Bar "Heat Map" is an overview of hot spots

Click jump to scroll Asm



## Timeline Visualizes Thread Behavior

Intel<sup>®</sup> VTune<sup>™</sup> Amplifier



Optional: Use API to mark frames and user tasks Frame Suser Task



Optional: Add a mark during collection



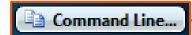
## Command Line Interface

Automate analysis

#### amplxe-cl is the command line:

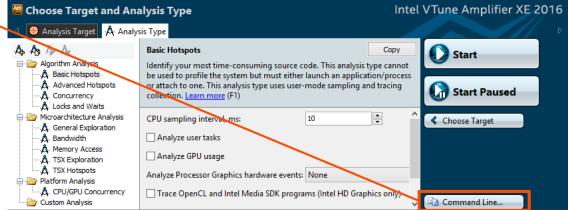
- Windows: C:\Program Files (x86)\Intel\VTune Amplifier XE \bin[32|64]\amplxe-cl.exe
- Linux: /opt/intel/vtune amplifier xe/bin[32|64]/amplxe-cl

Help: amplxe-cl -help Command Line...



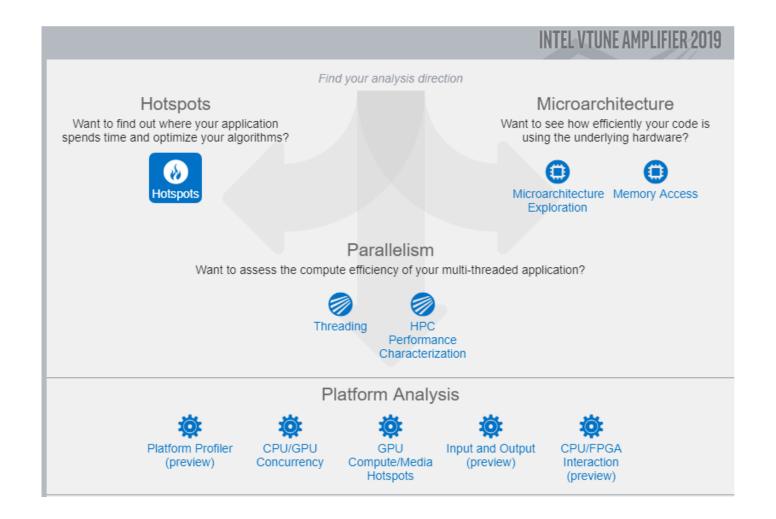
#### Use UI to setup

- 1) Configure analysis in UI
- 2) Press "Command Line..." button
- 3) Copy & paste command



Great for regression analysis – send results file to developer Command line results can also be opened in the UI

## VTune Predefined Analyses



## VTune Command Line Analysis Configuration

How to Run VTune on MPI Applications

```
><mpi_launcher> - n N <vtune_command_line> ./app_to_run
```

- >srun –n 48 -N 16 amplxe-cl –collect memory-access –trace-mpi –r result\_dir ./my\_mpi\_app
- >mpirun –n 48 -ppn 16 amplxe-cl –collect hotspots –r result\_dir ./my\_mpi\_app
- Encapsulates ranks to per-node result directories suffixed with hostname
  - result\_dir.hostname1 with 0-15, result\_dir.hostname2 with 16-31, result\_dir.hostname3 with 32-47
- Add **-trace-mpi** option for VTune CL to enable per-node result directories for non-Intel MPIs
- Works for software and Intel driver-based collectors

## VTune Command Line Analysis Configuration

Selective Rank Profiling

Superposition of application to launch and VTune command line for selective ranks to reduce trace size

Example: profile rank 1 from 0-15:

>mpirun -n 1 ./my\_app : -n 1 <vtune\_command\_line> -- ./my\_app : -n 14 ./my\_app

• In the case of Intel MPI launcher –gtool option can be used:

Example: profile ranks 3, 7, 11-13 from 0-15:

>mpirun –gtool "amplxe-cl –collect advanced-hotspots –r result\_dir:3,7,11-13" ./my\_app

#### Finalization on KNL

Result finalization and viewing on KNL target might be slow Use the recommended workflow:

1. Run collection on KNL deferring finalization to host:

>amplxe-cl -collect memory-access -no-auto-finalize -r <my\_result\_dir> ./my\_app

- 2. Finalize the result on the host
  - Provide search directories to the binaries of interest for resolving with –search-dir option

```
>amplxe-cl -finalize -r <my_result_dir> -search-dir <my_binary_dir>
```

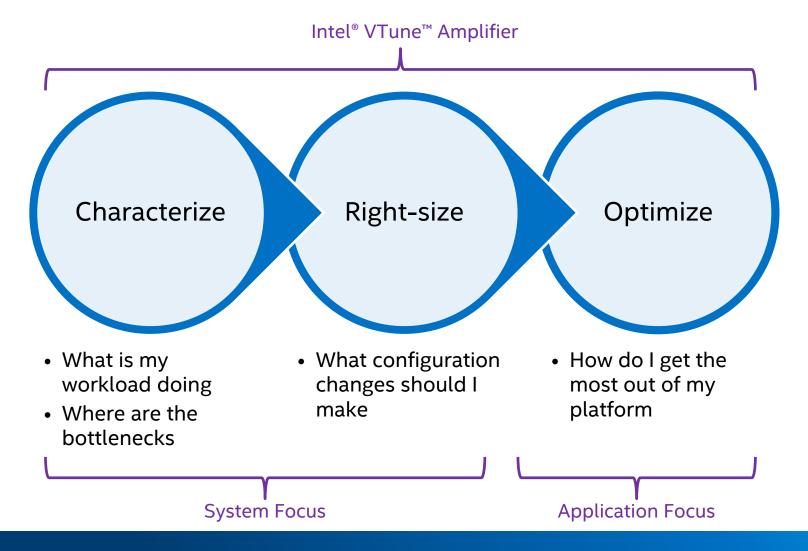
3. Generate reports, work with GUI

>amplxe-cl -report hotspots -r <my\_result\_dir>

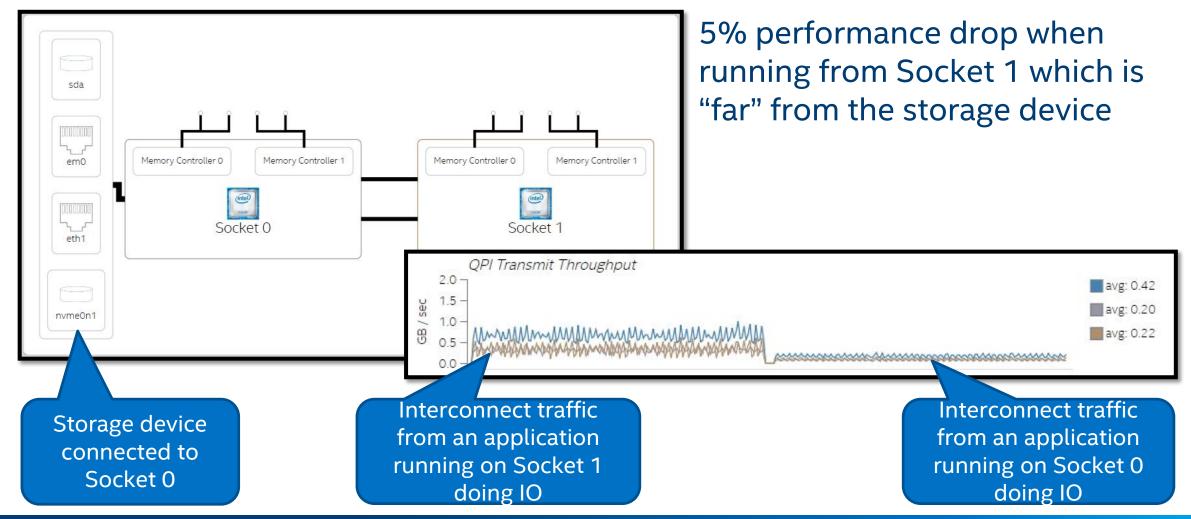


# INTEL VTUNE AMPLIFIER PLATFORM PROFILER

## 3-steps for optimizing complex workloads

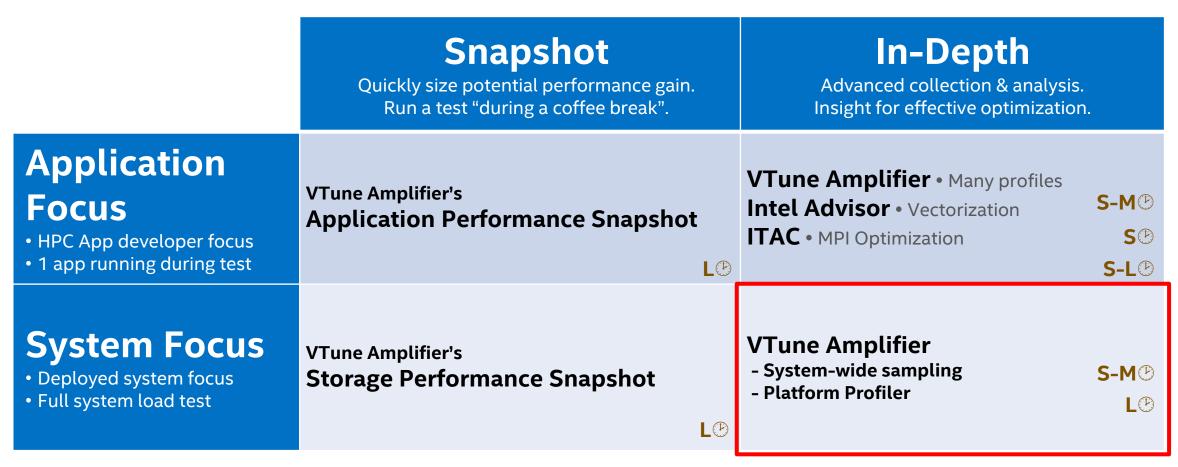


## **Configuration Matters!**



## The Long & Short of Performance Analysis

Get the big picture first with a Snapshot or Platform Profiler



Maximum collection times: Leelong (hours) Meemedium (minutes) Seeshort (seconds-few minutes)

Identify system performance & configuration issues and headroom

#### Target User

- Infrastructure Architects
- Software Architects & QA



#### Analyze performance

- Display current configuration
- ~150 hardware and ~20 OS metrics

#### Identify system configuration issues

- Inefficient memory module placements
- Need for faster storage, larger/faster memory

#### Identify potential software issues

- Inefficient CPU/storage/memory utilization
- Near vs. far memory accesses (NUMA)

#### Common use cases

#### Visualize workload behavior

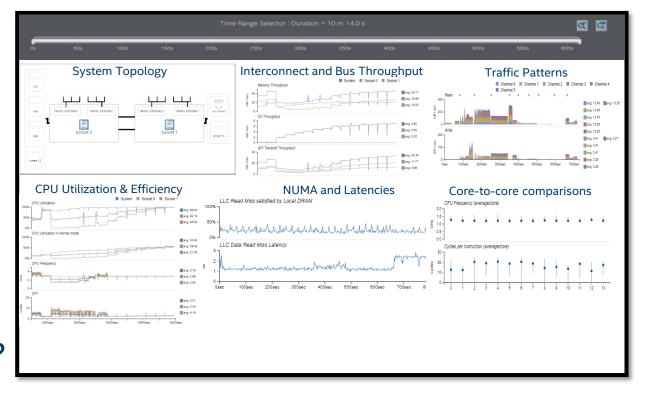
- Very low overhead ~2%
- Long running workloads (hours)

#### Plan tuning strategy

- Which app needs it most?
- Which phase of the app?
- Optimize cache? I/O? Threading?

#### Optimize hardware configuration

Add more I/O? Add memory?



Progressive disclosure methodology

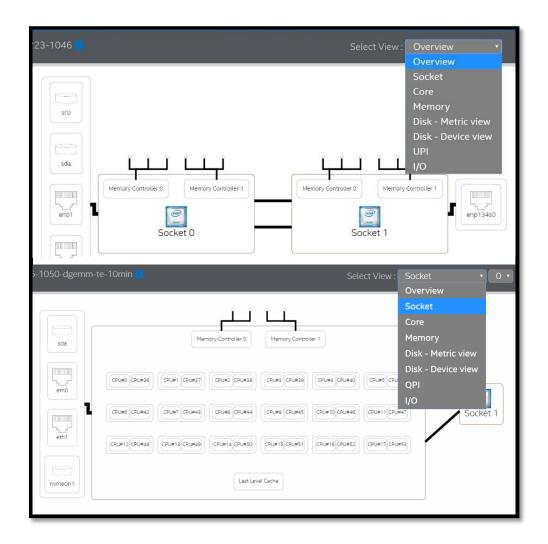
Start with Overview and Topology

View different aspects of system

Socket, Core, Memory, Disk, UPI, I/O

#### Drill down

- Socket → Core → Internal Caches
- Socket → Memory Link → Memory Module



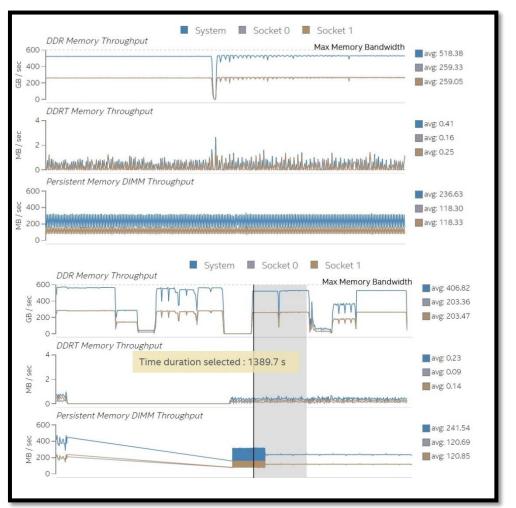
Telemetry data collected (and displayed) at a granularity of 100ms

Analyze hours of execution

- No process-level info
- Average won't hide erratic behavior

Select and zoom to desired execution region

 All graphs and averages adjust to selection)



#### Data collection

#### **Data Collector**

## Platform Profiler Analysis





#### Data Collection "Targets"

- Windows\*
- Linux\*

#### Analysis and visualization

- Web-based UI
- Works best with Chrome

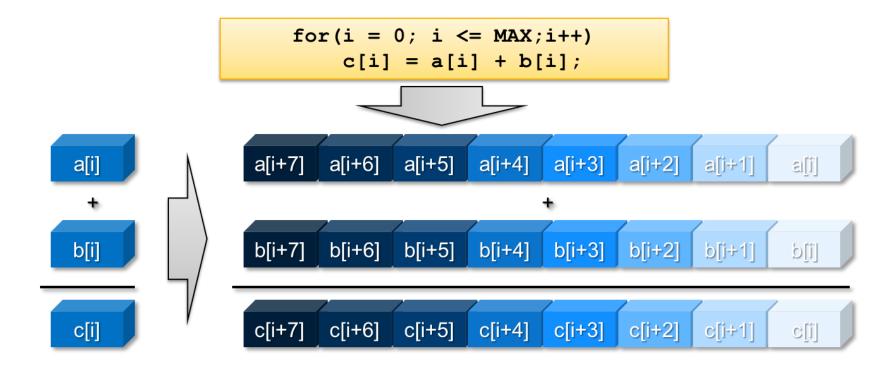


# INTEL® ADVISOR

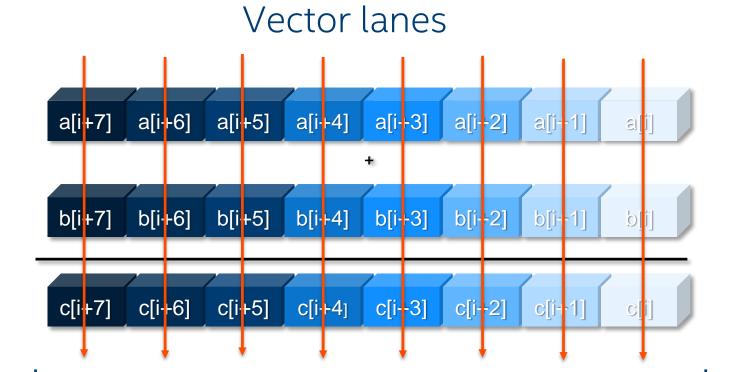
#### Vectorization of code

Transform sequential code to exploit vector processing capabilities (SIMD) of Intel processors

- Manually by explicit syntax
- Automatically by tools like a compiler



#### Vectorization terms



Vector length(VL): Elements of the vector

All elements of vector are of the same data types

## Many Ways To Vectorize

**Compiler:** 

**Auto-vectorization (no change of code)** 

**Compiler:** 

Auto-vectorization hints (#pragma vector, ...)

**Compiler:** 

OpenMP\* 4.0

**SIMD** intrinsic class

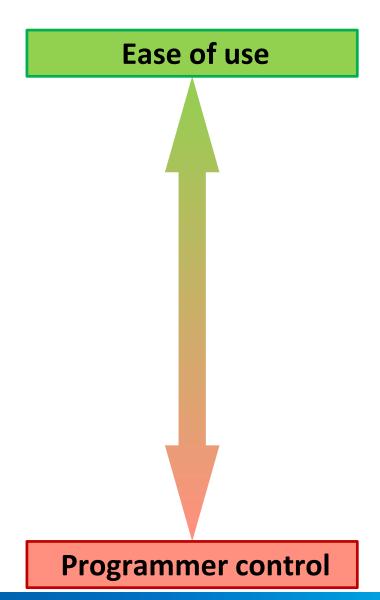
(e.g.: F32vec, F64vec, ...)

**Vector intrinsic** 

(e.g.: \_mm\_fmadd\_pd(...), \_mm\_add\_ps(...), ...)

Assembler code

(e.g.: [v]addps, [v]addss, ...)



## Tuning for Skylake - Compiler options

Both Skylake and Knights Landing processors have support for Intel® AVX-512 instructions. There are three ISA options in the Intel® Compiler:

```
-xCORE-AVX512: Targets Skylake, contains instructions not supported by Knights Landing
```

-xCOMMON-AVX512 : Targets both Skylake and Knights Landing

-xMIC-AVX512 : Targets Knights Landing, includes instructions not supported by Skylake

Intel® Compiler is conservative in its use of ZMM (512bit) registers so to enable their use with Skylake the additional flag -qopt-zmm-usage=high must be set.

## Validating Vectorization Success I: Compiler report

- -qopt-report[=n]: tells the compiler to generate an optimization report
  - n: (Optional) Indicates the level of detail in the report. You can specify values 0 through 5. If you specify zero, no report is generated. For levels n=1 through n=5, each level includes all the information of the previous level, as well as potentially some additional information. Level 5 produces the greatest level of detail. If you do not specify n, the default is level 2, which produces a medium level of detail.
- -qopt-report-phase[=list]: specifies one or more optimizer phases for which optimization reports are generated.
  - loop: the phase for loop nest optimization
  - vec: the phase for vectorization
  - par: the phase for auto-parallelization
  - all: all optimizer phases
- -qopt-report-filter=string: specified the indicated parts of your application, and generate optimization reports for those parts of your application.

## Validating Vectorization Success II

- -S: assembler code inspection
  - Most reliable way and gives all details of course
  - Check for scalar/packed or (E)VEX encoded instructions:
     Assembler listing contains source line numbers for easier navigation
  - Compiling with -qopt-report-embed (Linux\*, macOS\*) helps interpret assembly code
- Performance validation
  - Compile and benchmark with -no-vec -qno-openmp-simd or on a loop by loop basis via #pragma novector or !DIR\$ NOVECTOR
  - Compile and benchmark with selected SIMD feature
  - Compare runtime differences

### Intel® Advisor

#### Boosting your application by threading and vectorization

#### **Compiler will not always vectorize**

- Check for Loop Carried Dependencies using Intel® Advisor
- All clear? Force vectorization.
   C++ use: pragma simd, Fortran use: SIMD directive

Arrays of structures are great for intuitively organizing data, but are much less efficient than structures of arrays. Use the Intel® SIMD Data Layout Templates (Intel® SDLT) to map data into a more efficient layout for vectorization.

#### Not all vectorization is efficient vectorization

- Stride of 1 is more cache efficient than stride of 2 and greater. Analyze with Intel® Advisor.
- Consider data layout changes
   Intel<sup>®</sup> SIMD Data Layout Templates can help

#### Get Faster Code Faster! Intel® Advisor

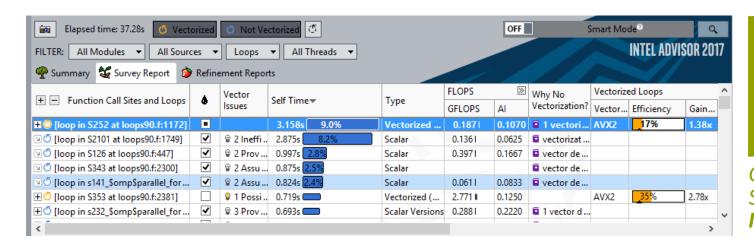
#### **Vectorization Optimization**

#### Have you:

- Recompiled for AVX2 with little gain
- Wondered where to vectorize?
- Recoded intrinsics for new arch.?
- Struggled with compiler reports?

#### **Data Driven Vectorization:**

- What vectorization will pay off most?
- What's blocking vectorization? Why?
- Are my loops vector friendly?
- Will reorganizing data increase performance?
- Is it safe to just use pragma simd?

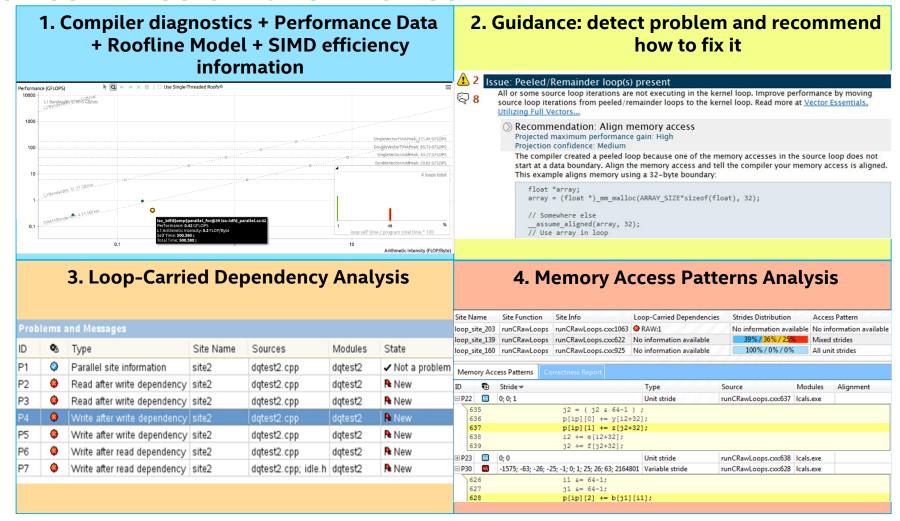


"Intel® Advisor's Vectorization Advisor permitted me to focus my work where it really mattered. When you have only a limited amount of time to spend on optimization, it is invaluable."

Gilles Civario
Senior Software Architect
Irish Centre for High-End Computing

## 4 Steps to Efficient Vectorization

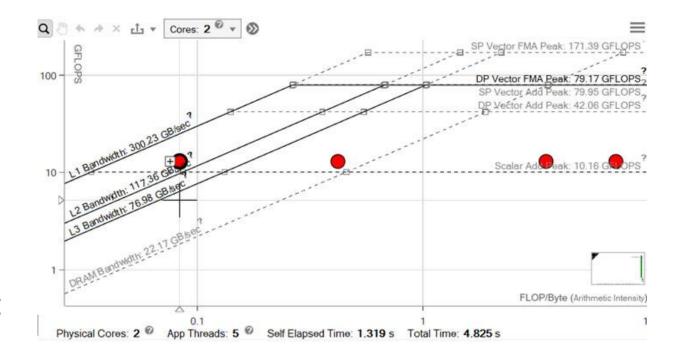
#### Intel® Advisor – Vectorization Advisor



## Integrated Roofline model

In the Intel® Advisor Integrated Roofline chart the Arithmetic Intensity and memory traffic for each level of the memory hierarchy is represented separately.

You can visualize the levels that need further optimization.

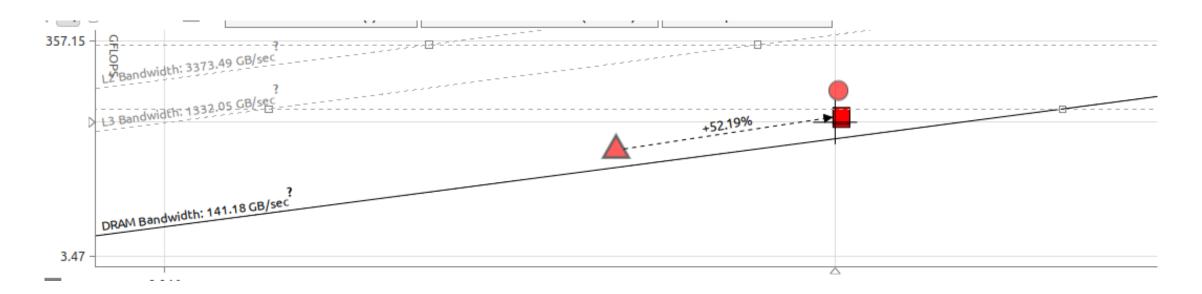




## Roofline compare

Visualize multiple roofline charts on the same graph.

Test optimization strategies and see how much progress your are making.





## New and Improved Summary

#### 

Elapsed Time 7.71s

Vector Instruction Set AVX2, AVX

Number of CPU Threads 36

#### ○ Performance characteristics

Metrics
Total CPU time

Time in 2 vectorized loops

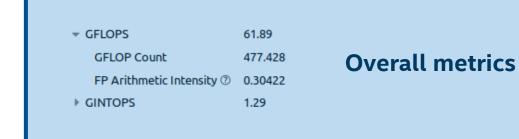
Time in scalar code

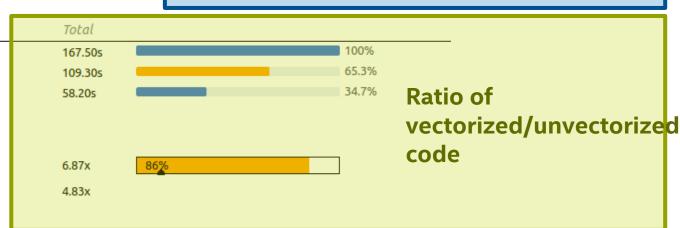
∀ Vectorization Gain/Efficiency

Vectorized Loops Gain/Efficiency®

Program Approximate Gain ?

**⊙** OP/S and Bandwidth

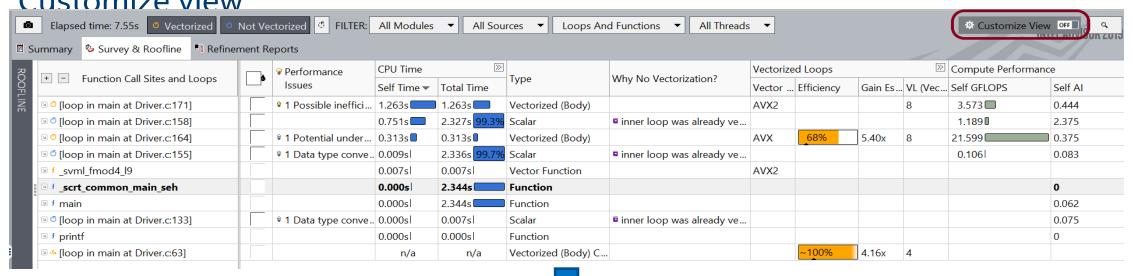


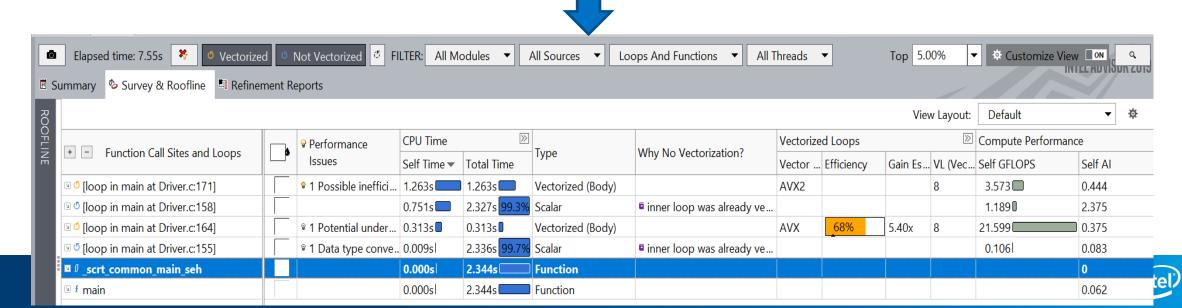


Effective OP/S And Bandwidth	Utili	lization :	🗘 Hardware Peak		
> GFLOPS	<b>61.89</b> 4.7% 2.3%		1318 (DP) FLOPS 2646 (SP) FLOPS		-
> GINTOPS	<b>1.292</b> 0.19% 0.097%		662.8 (Int64) INTOPS 1326 (Int32) INTOPS	Informations on Operations and	Memory transfers
> CPU <-> Memory [L1+NTS GB/s]	<b>203.4</b> 1.6%	out of '	12370 GB/s [bytes]	miormations on operations and	ricinory transfers
> L2 Bandwidth [GB/s]	<b>105.9</b> 3.1%	out of 3	3374 GB/s [cacheline bytes]		
> L3 Bandwidth [GB/s]	<b>69.07</b> 5.2%	out of '	1332 GB/s [cacheline bytes]		
> DRAM Bandwidth [GB/s]	<b>14.88</b> 11%	out of '	141.2 GB/s [cacheline bytes]		(intel)

## Column Configurator







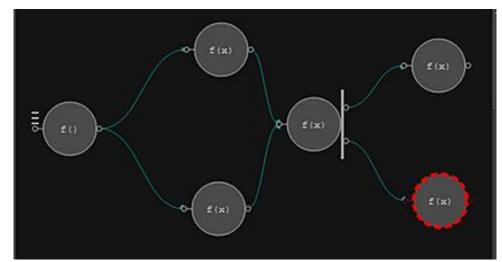
## Visualize Parallelism—Interactively Build, Validate & Analyze Algorithms

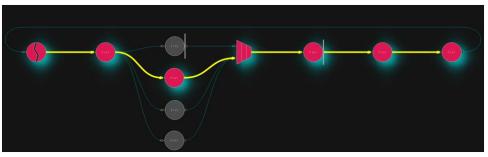
Intel® Advisor—Flow Graph Analyzer (FGA) Design mode

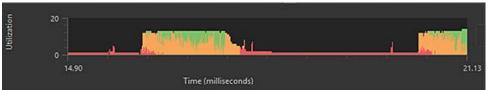
- Allows you to create a graph topology interactively
- Validate the graph and explore what-if scenarios
- Add C/C++ code to the node body
- Export C++ code using Threading Building Blocks (TBB) flow graph
   API

#### Analysis mode

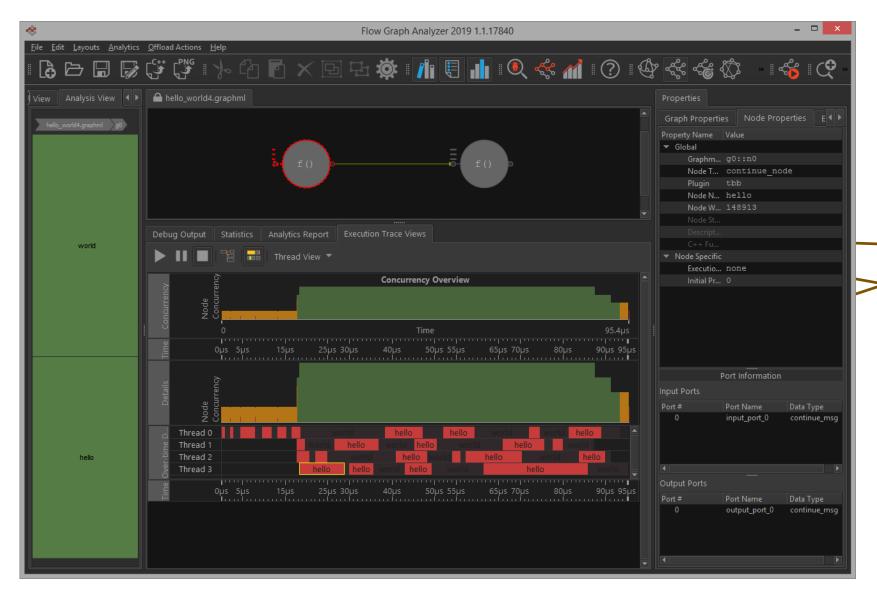
- Compile your application (with tracing enabled)
- Capture execution traces during the application run
- Visualize/analyze in Flow Graph Analyzer







#### Intel® Advisor – Flow Graph Analyzer (Analysis mode)



Trace program execution

Show correlation

Trace Playback

#### How to set it up (command line)?

#### Before running an analysis, run:

- \$ export ADVIXE\_EXPERIMENTAL=int\_roofline
- Use –integrated option

#### Run the survey

advixe-cl -collect survey -integrated ...... -- ./my\_application param1 param2 ...

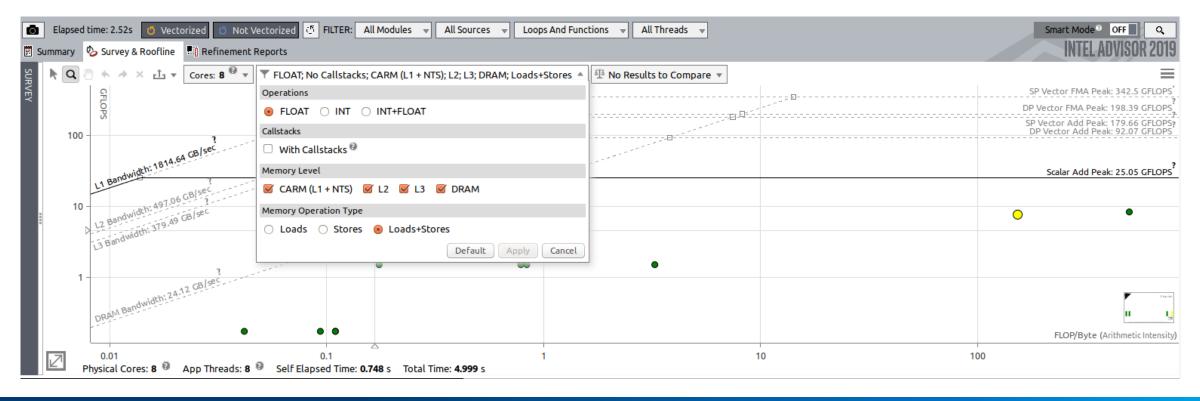
#### Run the trip count and flop

- advixe-cl –collect tripcounts -flop –integrated -enable-cache-simulation ...... -- ./my\_application param1 param2 ...
- Or Run Roofline analysis
- advixe-cl –collect roofline -integrated... -- ./my\_application param1 param2



## How to display the Integrated Roofline chart

You can select which memory level you want to display. Each memory level selected display an additional dot for every kernel. Each dot of the same kernel has the same performance but different Arithmetic Intensities. Here we selected CARM, L2, L3 and DRAM



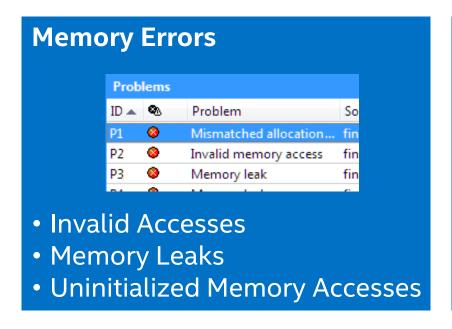


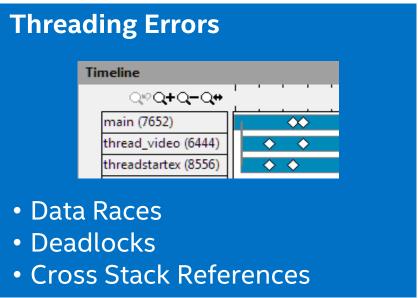


## INTEL® INSPECTOR

Memory and thread debugger

## Motivation for Intel® Inspector





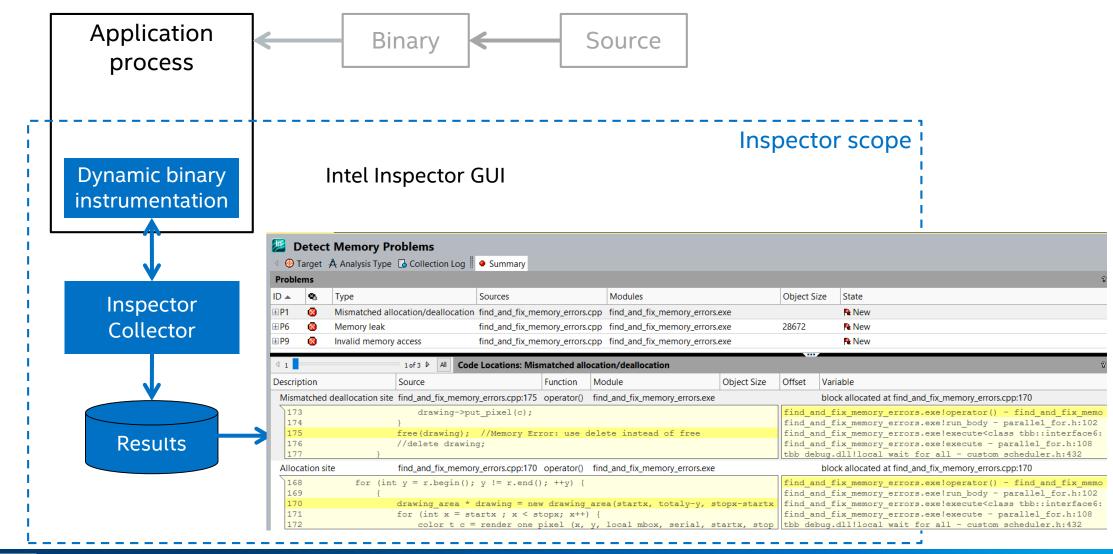
#### Multi-threading problems

- Hard to reproduce,
- Difficult to debug
- Expensive to fix

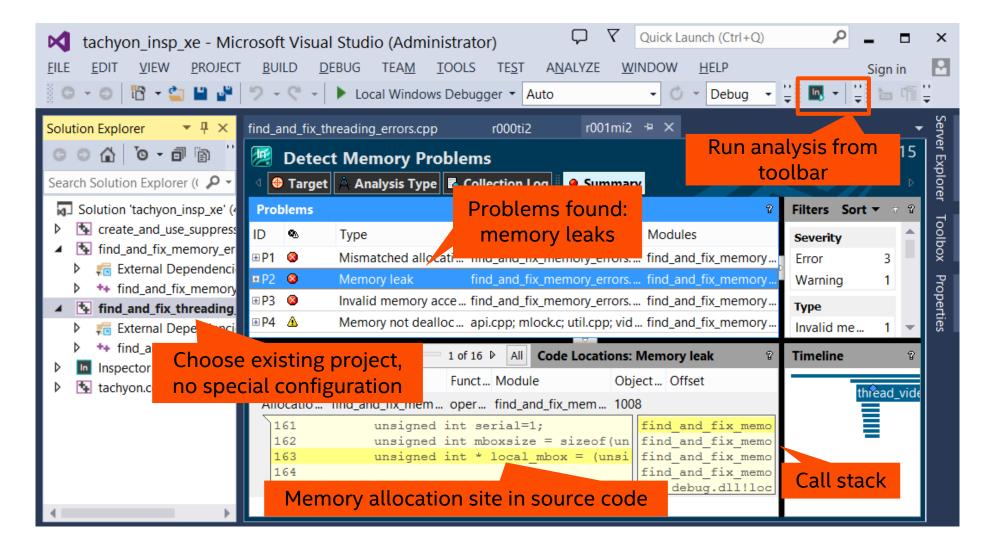


Let the tool do it for you

## Intel® Inspector: Dynamic Analysis

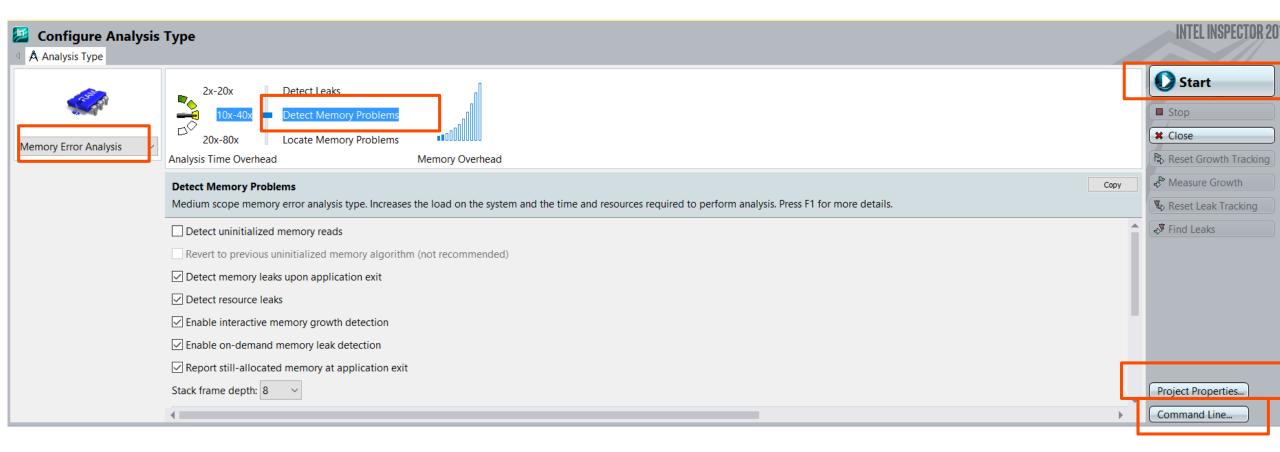


## How it Looks: Visual Studio\* Integration

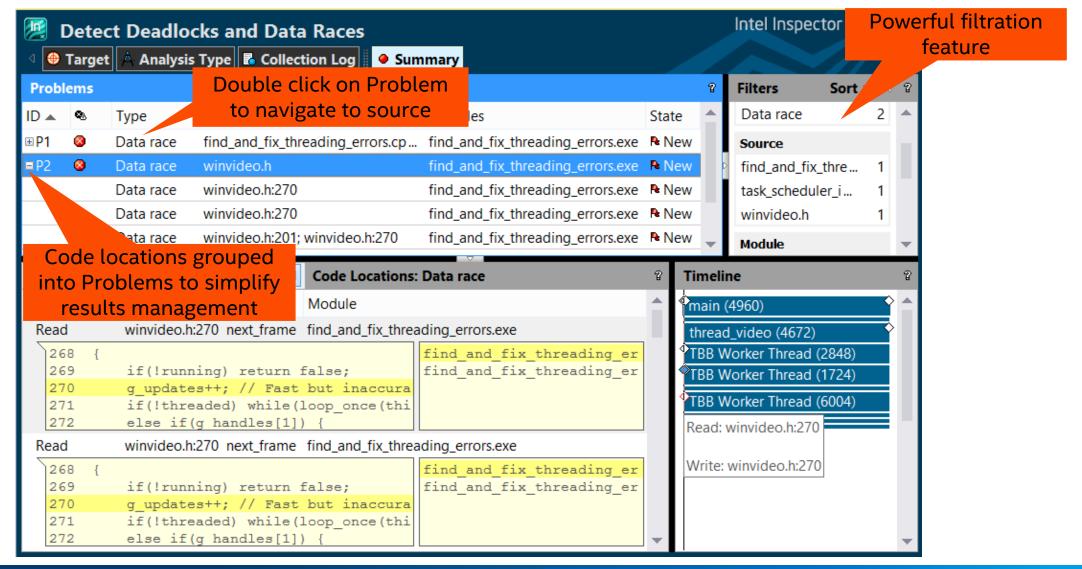




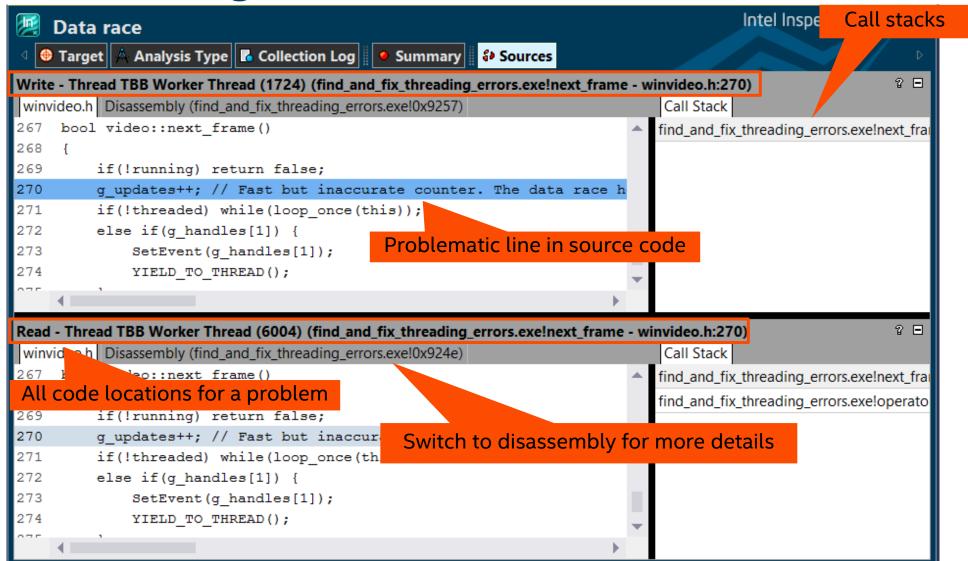
#### Standalone GUI: Windows\* and Linux\*



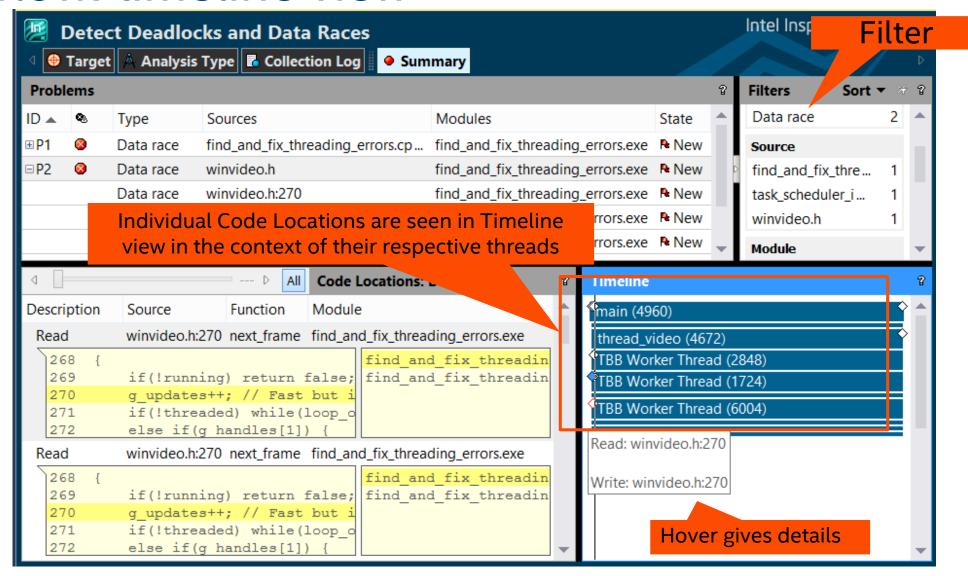
## Workflow: manage results



## Workflow: navigate to sources



#### Workflow: timeline view



**Analyze Memory Growth** 



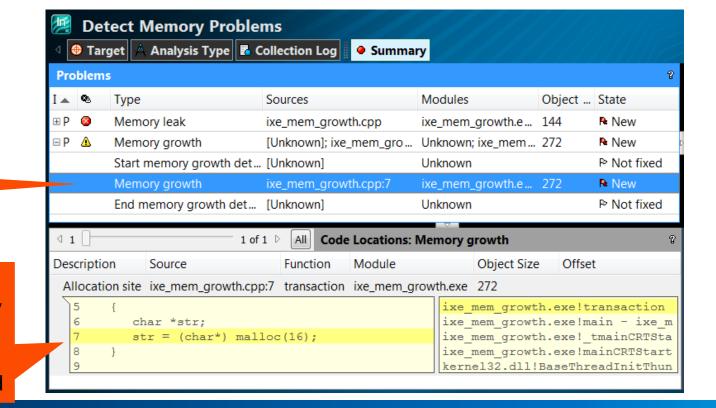
**Analysis Results:** 

Memory Growth Problem Set

Code location for each block of memory that was allocated but not de-allocated during the time period **During Analysis:** 

**Set Start Point** 

**Set End Point** 

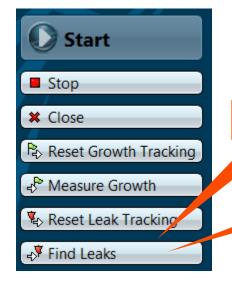


#### On-demand leak detection

Set Start

Set End Point

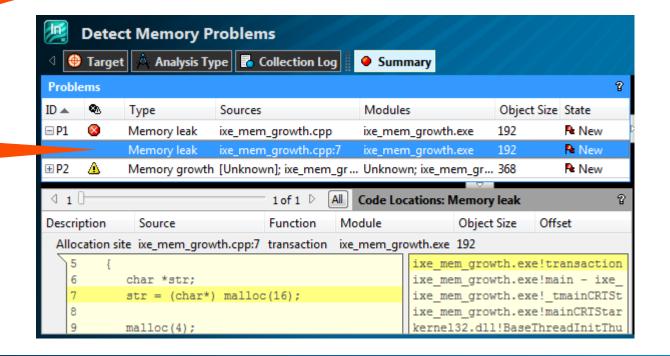
**Point** 



- Check code regions between points
   'A' and 'B' for leaks
- Check daemon processes for leaks
- Check crashing processes for leaks

#### Analysis Results:

Memory Leak shown during run time



#### Define analysis scope in source code

```
#include <ittnotify.h>
void ProcessPipeline()
   __itt_heap_reset_detection(__itt_heap_leaks); // Start measuring memory leaks
   DoSomeOtherWork();
   itt heap reset detection( itt heap growth); // Start measuring memory growth
   pipeline stage2();
                                                          // Run
   pipeline stage 2
   itt heap record( itt heap growth);  // Report memory growth in
   stage 2
```

## Correctness analyses overhead

#### Inspector XE tracks

- Thread and Sync APIs
- Memory accesses

#### Inspector performs binary instrumentation using PIN

- Dynamic instrumentation system provided by Intel (<a href="http://www.pintool.org">http://www.pintool.org</a>)
- Injected code used for observing the behavior of the running process
- Source modification/recompilation is not needed



Increases execution time and memory consumed (potentially significantly)

The Inspector XE dilates both time and memory consumed significantly!

## Workload guidelines

#### Use small data set

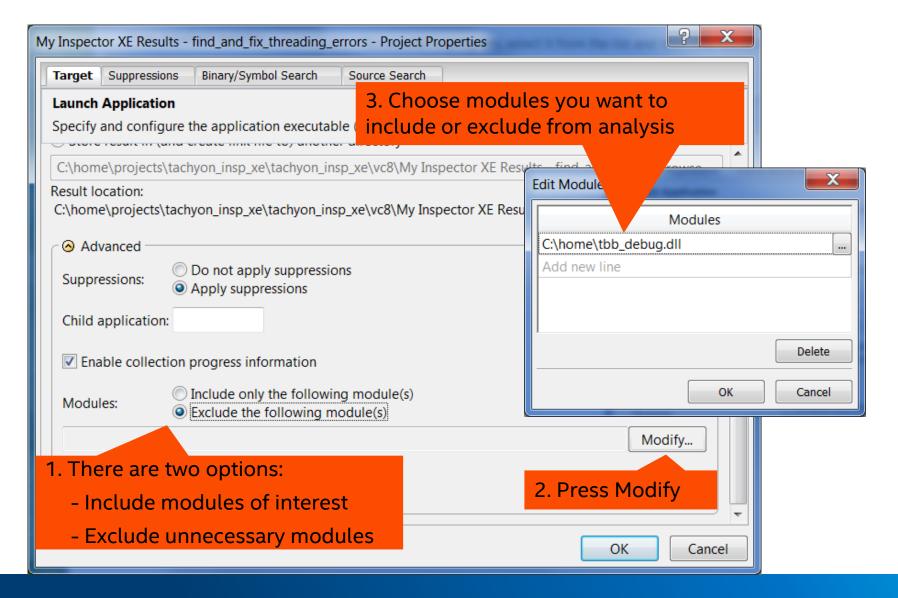
- Smaller number of threads
- Minimize data set size (e.g. smaller image sizes)
- Minimize loop iterations or time steps
- Minimize update rates (e.g. lower frames per second)

#### Use small but representative data set

Only actually executed code paths are analyzed

Scale down workload to speed up analysis!

#### Include and Exclude modules



## Debugger integration

#### Break into debugger

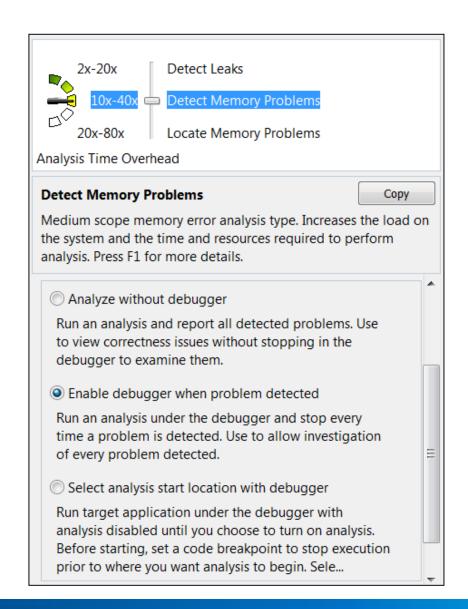
- Analysis can stop when it detects a problem
- User is put into a standard debugging session

#### Windows\*

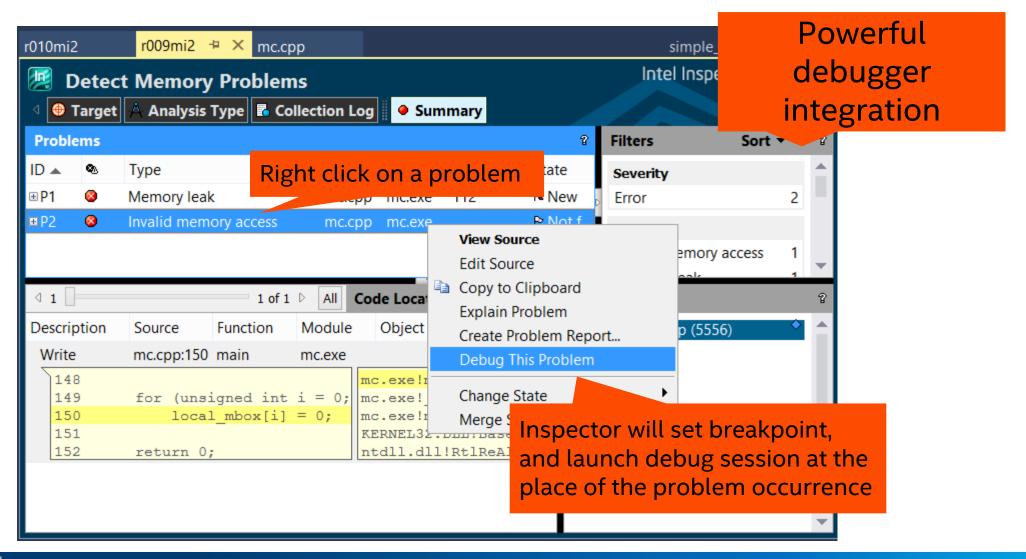
Microsoft\* Visual Studio Debugger

#### Linux\*

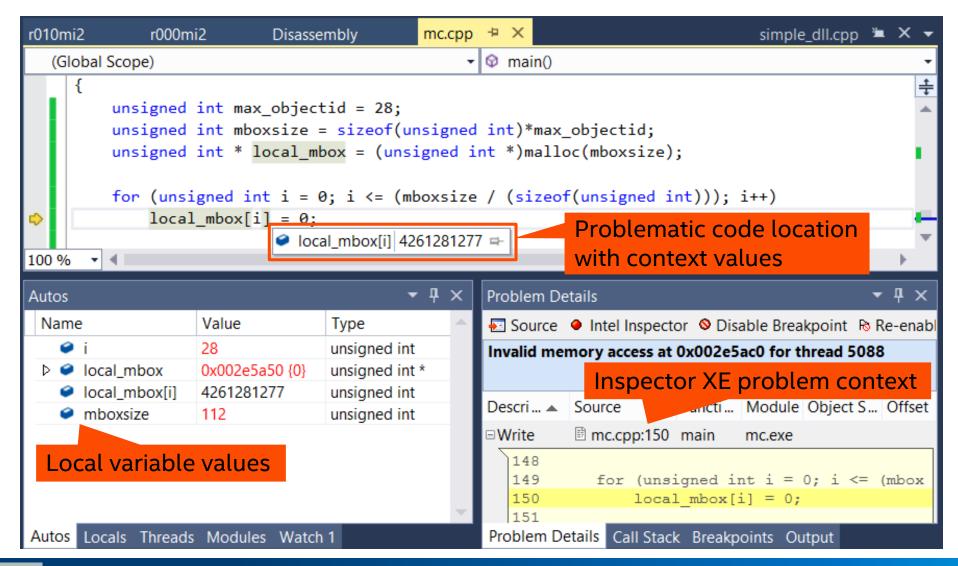
gdb



## Debug this problem



#### Debug this problem



#### Collect results and create baseline

```
inspxe-cl -collect mi1 -r r002mi1 -- D:\tests\my_app.exe
inspxe-cl -collect mi1
-module-filter module1.dll,module2.dll -module-filter-
  mode exclude -- D:\tests\my_app.exe
inspxe-cl -collect mi1 -executable-of-interest
  mem_error.exe -- D:\tests\startup_script.bat
inspxe-cl -create-suppression-file "D:\tests\mySup"
  -result-dir r002mi1
inspxe-cl -collect mi1 -suppression-file "D:\tests\mySup"
  -- D:\tests\my_app.exe
inspxe-cl -collect mi1 -baseline-result mi1_base --
  D:\tests\my_app.exe
```

#### Intel Inspector: User APIs

#### Enable you to

- Control collection, limit analysis scope
- Specify non-standard synchronization primitives
- Specify custom memory allocation primitives

#### To use user APIs:

- Include ittnotify.h, located at <install\_dir>/include
- Insert <u>\_\_itt</u>\* notifications in your code
- Link to the libittnotify.lib file located at <install\_dir>/ <lib32|lib64>
- Available for C/C++ and Fortran



#### Collection control APIs

API	Description
<pre>voiditt_suppress_push(    unsigned int etype)</pre>	Stop analyzing for errors on the current thread
<pre>voiditt_suppress_pop (   void)</pre>	Resume analysis
<pre>voiditt_suppress_mark_range (    itt_suppress_mode_t mode,     unsigned int etype,     void * address,     size_t size);</pre>	Suppress or unsuppress error detection for the specific memory range (object).
<pre>voiditt_suppress_clear_range (    itt_suppress_mode_t mode,     unsigned int etype,     void * address,     size_t size);</pre>	Clear the marked memory range

## Using the Intel® Inspector with MPI

Compile the inspector\_example.c code with the MPI scripts

Use the command-line tool under the MPI run scripts to gather report data

```
mpirun -n 4 inspxe-cl --result-dir insp_results
   -collect mi1 -- ./insp_example.exe
```

Output is: a results directory for each MPI rank in the job

```
ls | grep inspector_results on Linux
```

Launch the GUI and view the results for each particular rank

```
inspxe-gui inspector_results.<rank#> on Linux
```



# INTEL® PARALLEL STUDIO XE CLUSTER EDITION OVERVIEW

For Distributed Performance

# **Cluster Tools**

#### Intel® Parallel Studio XE

Profiling, Analysis, and Architecture

Intel® Inspector

Memory and Threading Checking

Intel® VTune™ Amplifier

Performance Profiler

Performance Libraries Intel® Data Analytics Acceleration Library
Optimized for Data Analytics & Machine Learning

Intel® Math Kernel Library

Optimized Routines for Science, Engineering, and Financial

Intel® Advisor

Vectorization Optimization and Thread Prototyping

Intel® Cluster Checker
Cluster Diagnostic Expert System

Intel® Trace Analyzer and Collector

MPI Profiler

Intel® MPI Library

Intel® Integrated Performance Primitives
Image, Signal, and Compression Routines

Intel® Threading Building Blocks
Task-Based Parallel C++ Template Library

Intel® C/C++ and Fortran Compilers

Intel® Distribution for Python

Performance Scripting

Boost Distributed Application Performance with Intel® MPI Library

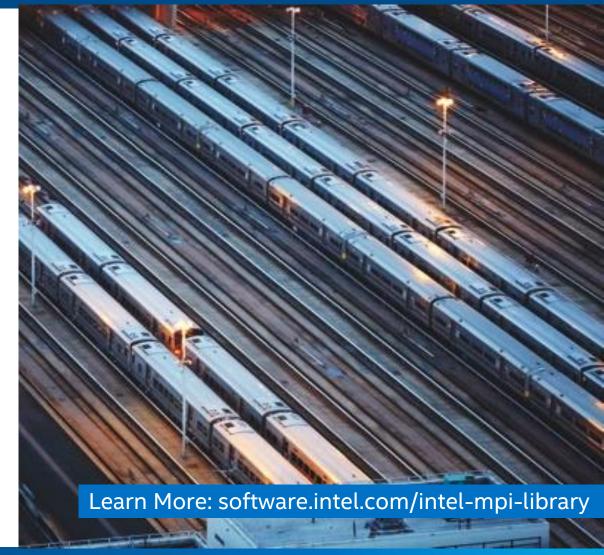
Performance, Scalability & Fabric Flexibility

## Standards Based Optimized MPI Library for Distributed Computing

- Built on open source MPICH Implementation
- Tuned for low latency, high bandwidth & scalability
- Multi-fabric support for flexibility in deployment

#### What's New in 2019 Release

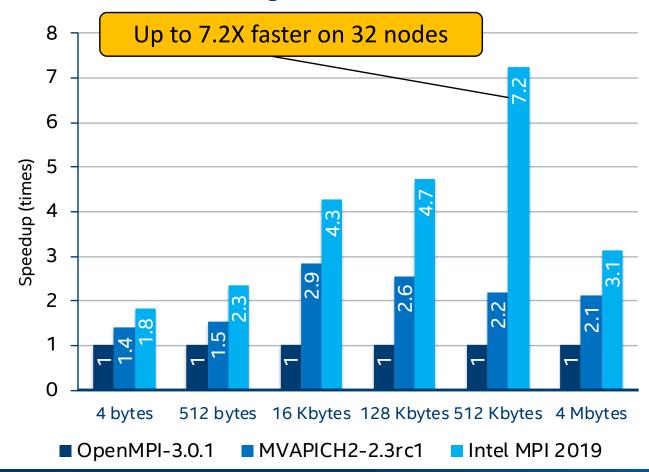
- New MPI code base- MPI-CH4 (on the path to Exascale & beyond)
- Greater scalability & shortened CPU paths
- Superior MPI Multi-threaded performance
- Supports the latest Intel® Xeon® Scalable processor



#### Superior MPI Performance with Intel® MPI Library 2019 on Linux\* 64

1,280 Processes, 32 Xeon nodes (Intel® Omni-Path) Linux\* 64

## Relative (Geomean) MPI Latency Benchmarks (Higher is Better)

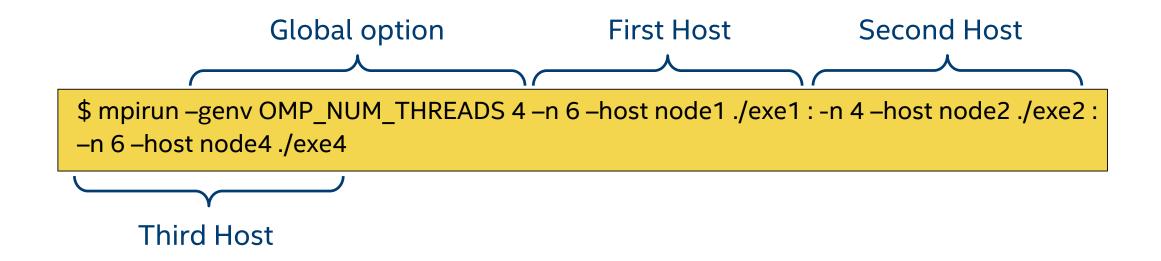


Performance results are based on testing as of Sept. 5, 2018 and may not reflect all publicly available security updates. See configuration disclosure for details. No product can be absolutely secure. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information, see <a href="PerformanceBenchmark Test Disclosure">PerformanceBenchmark Test Disclosure</a>.

Configuration: Testing by Intel as of Sept. 5, 2018.Hardware: Intel® Xeon®Gold 6148 CPU @ 2.40GHz; 192 GB RAM. Interconnect: Intel® Omni-Path Host Fabric InterfaceSoftware: RHEL\* 7.4; IFS 10.7.0.0.145; Libfabric internal; Intel® MPI Library 2019; Intel® MPI Benchmarks 2019 (built with Intel® C++ Compiler XE 18.0.2.199 for Linux\*);

Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessors dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice. Notice revision #20110804. For more complete information about compiler optimizations, see our Optimization Notice.

## Command Line Argument Set



May set both global and local variables for each host

No limit to number of different host or executables

For high numbers of hosts a configuration file is more convenient...

## **Configuration File**

Configuration file allows flexibility and automation

Notice commented out line – simple to change host assignment

```
$ cat theconfigfile
-genv OMP_NUM_THREADS 4
-n 6 -host node1 ./exe1
-n 4 -host node2 ./exe2
# -n 4 -host dead_node3 ./exe3
-n 6 -host node4 ./exe4
```

#### Launching job is straightforward

\$ mpirun -configfile theconfigfile

## Understanding MPI and Launcher Behavior

I\_MPI\_DEBUG=<level>

#### Debug Levels (cumulative):

- 0 *Default*, no debug information
- 1 Verbose error diagnostics
- 2 Fabric selection process
- 3 Rank, PID, node mapping
- 4 Process pinning [recommended]
- 5 Display Intel® MPI Library environment variables
- 6 Collective operation algorithm controls

I\_MPI\_HYDRA\_DEBUG=1

#### Turns on Hydra debug output

- Extremely verbose output
- Only turn on if needed

#### Fabric Selection (v2018 & earlier)

I\_MPI\_FABRICS=<intranode fabric>:<internode fabric> or <fabric>

- shm Shared Memory (only valid for intranode)
- dapl Direct Access Provider Library\*
- ofa Open Fabric Alliance (OFED\* verbs)
- tmi Tag Matching Interface
- tcp Ethernet/Sockets
- ofi OpenFabrics Interfaces\*

Default behavior goes through a list to find first working fabric combination If you specify a fabric, fallback is disabled, I MPI FALLBACK=1 to re-enable

## Fabric Selection (v2018 vs v2019)

I\_MPI\_FABRICS=<intranode fabric>:<internode fabric> or <fabric>

ofi – OpenFabrics Interfaces\*

Default behavior goes through a list to find first working fabric combination If you specify a fabric, fallback is disabled, I\_MPI\_FALLBACK=1 to re-enable

## Intel® MPI Support of Hybrid Codes

Intel® MPI is strong in mapping and pinning support for MPI processes

Sophisticated defaults or user controlled:

- For pure MPI codes use I MPI PIN PROCESSOR LIST
- For hybrid codes (default, takes precedence over I\_MPI\_PIN\_PROCESSOR\_LIST):

```
I_MPI_PIN_DOMAIN =<size>[:<layout>]
```

Defines mapping and pinning for MPI processes, leaves room for threads on remaining cores!

NB: Naturally extends to hybrid codes on Intel® Xeon Phi™

## **Default Binding**

```
$ export I MPI DEBUG=4
$ mpirun -machinefile ./hosts.txt -n 8 ./mpi hello
                                                                            Fabric provider
[0] MPI startup(): Multi-threaded optimized library
[0] MPID nem ofi init(): used OFI provider: psm2
   MPI startup(): shm and ofi data transfer modes
                                                                             Active transfer
                                                                                 modes
[0] MPI startup(): Rank Pid
                               Node name Pin cpu
                                          {0,1,2,3,4,5,6,7,8,9,40,41,42,43,44,45,46,47,48,49}
[0] MPI startup(): 0
                        121023 node0
[0] MPI startup(): 1
                        121024 node0
                                          {10,11,12,13,14,15,16,17,18,19,50,51,52,53,54,55,56,57,58,59}
[0] MPI startup(): 2
                        121025 node0
                                          {20,21,22,23,24,25,26,27,28,29,60,61,62,63,64,65,66,67,68,69}
[0] MPI startup(): 3
                        121026 node0
                                          {30,31,32,33,34,35,36,37,38,39,70,71,72,73,74,75,76,77,78,79}
[0] MPI startup(): 4
                        246334 node1
                                          {0,1,2,3,4,5,6,7,8,9,40,41,42,43,44,45,46,47,48,49}
[0] MPI startup(): 5
                                          {10,11,12,13,14,15,16,17,18,19,50,51,52,53,54,55,56,57,58,59}
                        246335 node1
[0] MPI startup(): 6
                                          {20,21,22,23,24,25,26,27,28,29,60,61,62,63,64,65,66,67,68,69}
                        246336 node1
[0] MPI startup(): 7
                        246337 node1
                                          {30,31,32,33,34,35,36,37,38,39,70,71,72,73,74,75,76,77,78,79}
Hi from MPI task 0
                                                      Equal distribution of cores among MPI ranks
```

## Using I\_MPI\_PIN\_PROCESSOR\_LIST

```
$ export I MPI DEBUG=4
$ export I MPI PIN PROCESSOR LIST=0,1,20,21
                                                                Fabric provider (no changes)
$ mpirun -machinefile ./hosts.txt -n 8 ./mpi hello
   MPI startup(): Multi-threaded optimized librar
   MPID nem ofi init(): used OFI provider: psm2
                                                                Active transfer modes (no changes)
   MPI startup(): shm and ofi data transfer modes
   MPI startup(): Rank Pid
                               Node name Pin cpu
   MPI startup(): 0
                        121023 node0
                                         {0}
   MPI startup(): 1 121024 node0
                                         {1}
   MPI startup(): 2
                    121025 node0
                                         {20}
                                                   Processes bound to specified CPUs, not floating
                     121026 node0
   MPI startup(): 3
                                         {21}
   MPI startup(): 4
                        246334 node1
                                         {0}
   MPI startup(): 5
                    246335 node1
                                         {1}
   MPI startup(): 6
                        246336 node1
                                         {20}
   MPI startup(): 7
                        246337 node1
                                         {21}
Hi from MPI task 0
```

### Using I\_MPI\_PIN\_DOMAIN

```
$ export I MPI DEBUG=4
                                                          Set binding to OMP range
$ export I MPI PIN DOMAIN=omp
$ export OMP NUM THREADS=10
$ mpirun -machinefile ./hosts.txt -n 8 ./mpi hello
[0] MPI startup(): Multi-threaded optimized library
[0] MPID nem ofi init(): used OFI provider: psm2
   MPI startup(): shm and ofi data transfer modes
[0] MPI startup(): Rank Pid
                              Node name Pin cpu
[0] MPI startup(): 0
                        121023 node0
                                         {0,1,2,3,4,40,41,42,43,44}
[0] MPI startup(): 1
                    121024 node0
                                        {5,6,7,8,9,45,46,47,48,49}
                                                                                     Each MPI task floats on
[0] MPI startup(): 2
                      121025 node0
                                        {10,11,12,13,14,50,51,52,53,54}
[0] MPI startup(): 3
                      121026 node0
                                        {15,16,17,18,19,55,56,57,58,59}
                                                                                      OMP_NUM_THREADS
[0] MPI startup(): 4
                      246334 node1
                                        {0,1,2,3,4,40,41,42,43,44}
                                                                                        logical processors
[0] MPI startup(): 5
                      246335 node1
                                        {5,6,7,8,9,45,46,47,48,49}
[0] MPI startup(): 6
                      246336 node1
                                        {10,11,12,13,14,50,51,52,53,54}
[0] MPI startup(): 7
                        246337 node1
                                         {15,16,17,18,19,55,56,57,58,59}
                                                                                      Careful in HT systems!
Hi from MPI task 0 OMP thread 0
```

### Intel® MPI Benchmarks 2019

# Standard benchmarks with OSI-compatible CPL license

- Enables testing of interconnects, systems, and MPI implementations
- Comprehensive set of MPI kernels that provide performance measurements for:
  - Point-to-point message-passing
  - Global data movement and computation routines
  - One-sided communications
  - File I/O
  - Supports MPI-1.x, MPI-2.x, and MPI-3.x standards

#### What's New:

### Introduction of new benchmarks

 Added benchmarks to test new multithreaded support (IMB-MT) and shared memory transport (IMB-P2P)

# Measuring Communication Speed with IMB

The simplest benchmark in IMB is called PingPong

Data packages of different size are sent from rank 0 to rank 1 and back:

```
$ mpirun -n 2 IMB-MPI1 pingpong
```

	= 2 		
#bytes	#repetitions	t[usec]	Mbytes/sec
0	1000	1.50	0.00
1	1000	1.49	0.67
2	1000	1.49	1.34
4	1000	1.47	2.71
8	1000	1.47	5.43
16	1000	1.69	9.46
32	1000	1.68	19.04
64	1000	1.67	38.22
128	1000	1.73	73.84
256	1000	1.75	146.12
512	1000	1.82	281.40
1024	1000	1.92	533.34
2048	1000	2.16	949.27
4096	1000	2.62	1561.88
8192	1000	3.60	2274.88
16384	1000	6.58	2490.74
32768	1000	8.58	3819.34
65536	640	16.51	3968.86
131072	320	21.15	6197.71
262144	160	32.07	8175.19
524288	80	54.01	9707.91
1048576	40	95.70	10956.77
2097152	20	181.25	11570.38
4194304	10	349.56	11998.90

# What is mpitune?

Tool to optimize Intel® MPI Library settings

Walks through [application specific] search space of settings and tests performance

Writes out a configuration file with the best settings found

Works in two different modes:

- Cluster Specific
- Application Specific

# Cluster Specific Tuning with mpitune

Find optimal values for library tuning knobs on the particular cluster or application environment.

- Run it once after installation and each time after a cluster configuration change
- Best configuration is recorded for each combination of communication device, number of nodes, MPI ranks and the process distribution model
- Configuration is stored in Intel ® MPI folders and available to all users

Collect configuration values: \$ mpitune [options]

Reuse recorded values: \$ mpirun –tune ./application

# Application Specific Tuning with mpitune

Find optimal values for library tuning knobs on the particular cluster or application environment

- Run it for each application and after application- or cluster configuration change
- Best configuration is recorded for each combination of communication device, number of nodes, MPI ranks and the process distribution model
- Configuration is stored in user's home

Collect configuration values:
\$ mpitune [options] \
 --application \"mpirun application\"

Reuse recorded values: \$ mpirun –tune ./app.conf \ ./application

# Example: Cluster Specific MPITUNE

MPITUNE is an executable script. The easiest way is to simply run:

```
$ mpitune
```

We may restrict MPITUNE on full nodes and the default fabric

```
$ mpitune -pr 8:8 -fl shm:dapl
```

hosts should be taken from provided hostfile or the batch system

As the search space is very wide, you may want to limit the number of minimum and maximum ranks per node as well as the number of nodes and the fabric used :

# MPITUNE – Output

Message size   Initial (bytes)   time	Tuibial	Times for algorithms					77-1: 4-4-4	77-1:3-4-3
	Alg 1	Alg 2	Alg 3	Alg 4	Tuned vs     initial (ex)	Validated     time	Validated v   initial (ex	
0	0.38	0.37	0.40	*0.35*	0.38	0.92X	0.39	1.03
4	3.46	*3.51*	51.77	13.81	3.45	1.01X	3.44	0.99
8	4.05	3.89*	52.01	13.78	*4.14	0.96X	4.02	0.99
16	4.00	<b> </b> *3.97*	52.04	13.98	4.47	0.99X	4.12	1.0
32	4.46	<b>*4.42</b> *	52.54	15.25	5.54	0.99X	4.41	0.9
64	4.85	<b>*4.84</b> *	52.88	16.29	8.22	1.00X	4.84	1.0
128	5.16	<b>  *5.15*</b>	52.98	17.29	11.47	1.00X	5.24	1.0
256	5.77	<b>*5.67</b>	54.86	8.04	25.84	0.98X	5.76	1.0
512	6.07	<b>*5.96</b>	54.89	8.42	26.49	0.98X	5.81	0.9
1024	9.14	*9.27	56.15	8.66*	27.60	0.95X	8.81	0.9
2048	11.03	*11.29	57.73	8.86*	29.85	0.80x	9.16	0.8
4096	11.26	*11.64	65.04	9.71*	33.99	0.86X	9.98	0.8
8192	18.05	*18.01	73.03	11.41*	41.31	0.63X	11.57	0.6
16384	28.02	*28.08	81.30	14.29*	55.85	0.51X	14.45	0.5
32768	50.47	*50.27	160.89	20.71*	61.36	0.41X	21.04	0.4
65536	93.98	*93.97	247.74	30.63*	82.26	0.33X	30.90	0.3
131072	163.70	*164.00	325.70	59.16*	136.41	0.36X	62.99	0.3
262144	460.85	742.38	<b>*470.05</b>	518.14	426.22*	0.92X	385.39	0.8
524288	823.88	1746.14	*818.26	1368.98	601.41*	0.73X	565.56	0.6
1048576	898.08	5993.07	3351.08	5261.42	*970.05*	1.08X	957.37	1.0
2097152	2003.62	14957.62	6862.75	13167.39	*2115.74*	1.06X	2104.40	1.0
4194304	3582.84	38222.43	*3671.79*	33904.29	4914.07	1.02X	3631.38	1.0
AVG	n/a	n/a	n/a	n/a	i n/a i	0.84X	n/a	0.8

### MPITUNE – Result File

```
$ cat mpiexec_shm_nn_1_np_32_ppn_32.conf

-genv I_MPI_ADJUST_BCAST '1:0-0;10:1-2;8:3-20;10:21-32;1:33-64;9:65-
192;10:193-2582;9:2583-4096;11:4097-25206;10:25207-65536;11:65537-
131072;9:131073-524288;10:524289-1048576;9:1048577-2715592;1:2715593-
2147483647'
-genv I_MPI_ADJUST_BARRIER '7'
-genv I_MPI_ADJUST_GATHER '1:0-1;4:2-12;1:13-64;4:65-947;3:948-2147483647'
```

Note that results files may be empty if the default settings are optimal.



# PROFILE & ANALYZE HIGH PERFORMANCE MPI APPLICATIONS WITH INTEL® TRACE ANALYZER & COLLECTOR 2019

Profile, Analyze & Visualize MPI Applications

Part of Intel® Parallel Studio XE Cluster Edition and Available Individually

# Intel® Trace Analyzer and Collector Overview

### Helps the developer to:

 Visualize and understand parallel application behavior

Evaluation

API and -tcollect ots

**Features** 

Event-based approach

Low overhead

Excellent scalability

Powerful aggregation and

Idealizer

Intel® Trace Collector

-trace

Trace File (.stf)

filtering functions

Intel® Trace Analyzer

Source Code

Compiler

Objects

Linker

Binary

Runtime

Output

# How to Use Intel® Trace Analyzer and Collector

It's Easy...

Step 1

Run your binary and create a tracefile:

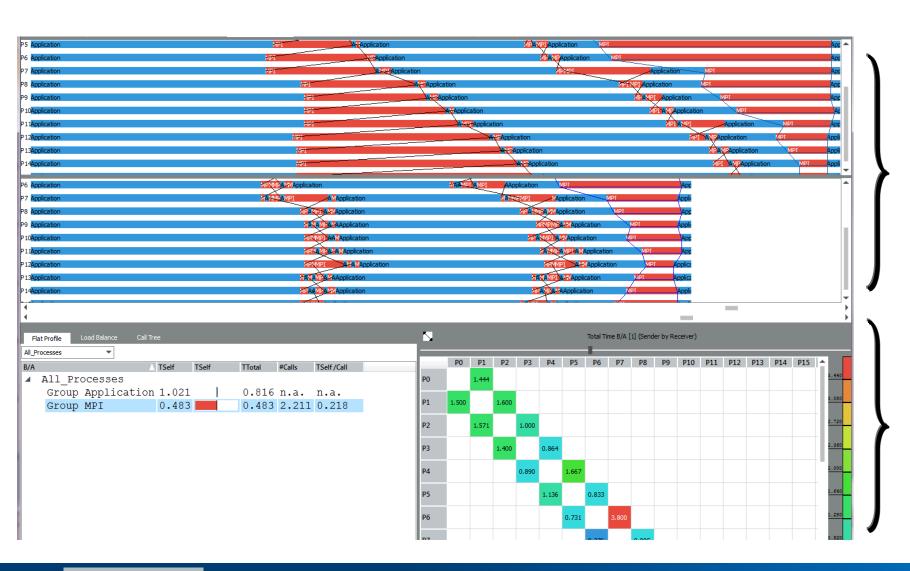
Step 2

View the results:

\$ traceanalyzer &

# Intel® Trace Analyzer and Collector



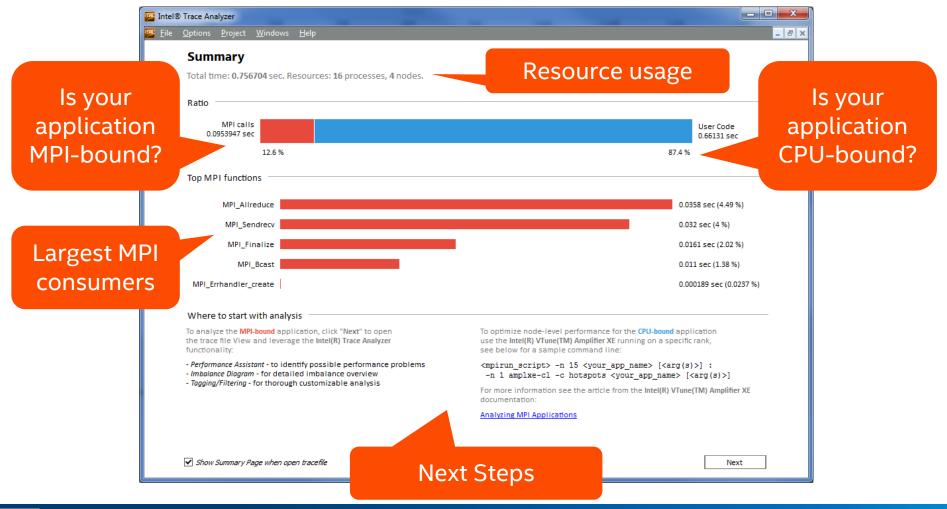


Compare the event timelines of two communication profiles

Blue = Computation Red = Communication

Chart showing how the MPI processes interact

# Summary page shows computation vs. communication breakdown



### Views and Charts

 Helps navigating through the trace data and keep orientation.

Every View can contain several Charts.

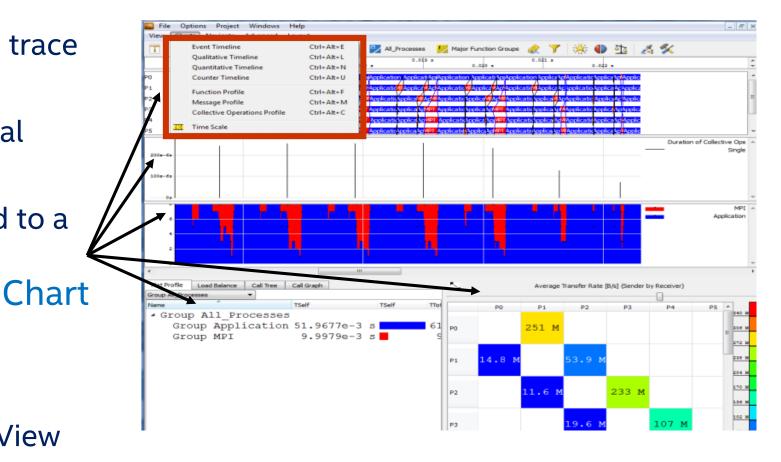
• All Charts in a View are linked to a single:

Time-span

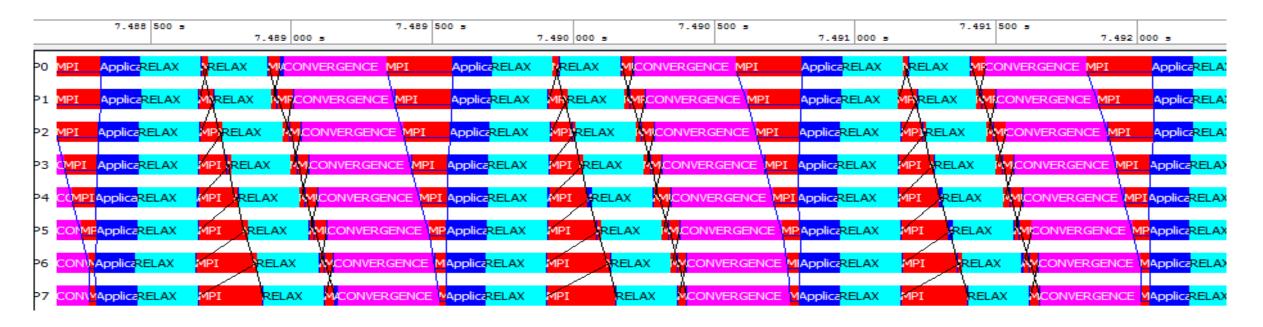
Set of threads

Set of functions

 All Charts follow changes to View (e.g., zooming)



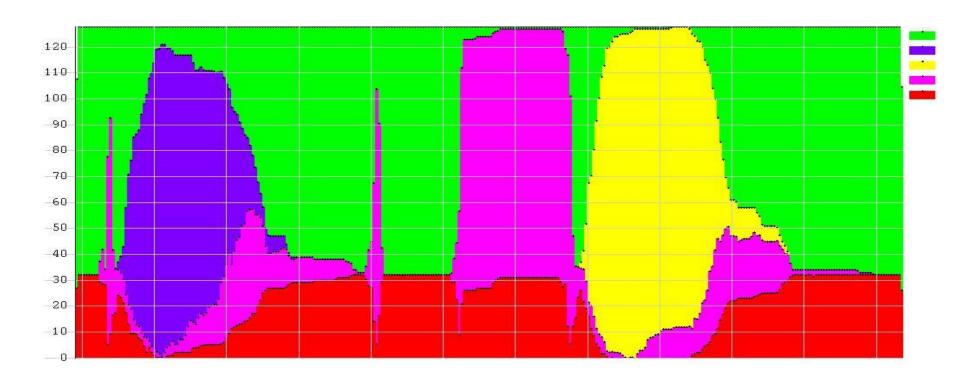
### **Event Timeline**



- Get detailed impression of program structure.
- Display functions, messages, and collective operations for each process/thread along time axis.
- Retrieve detailed event information.

### Quantitative Timeline

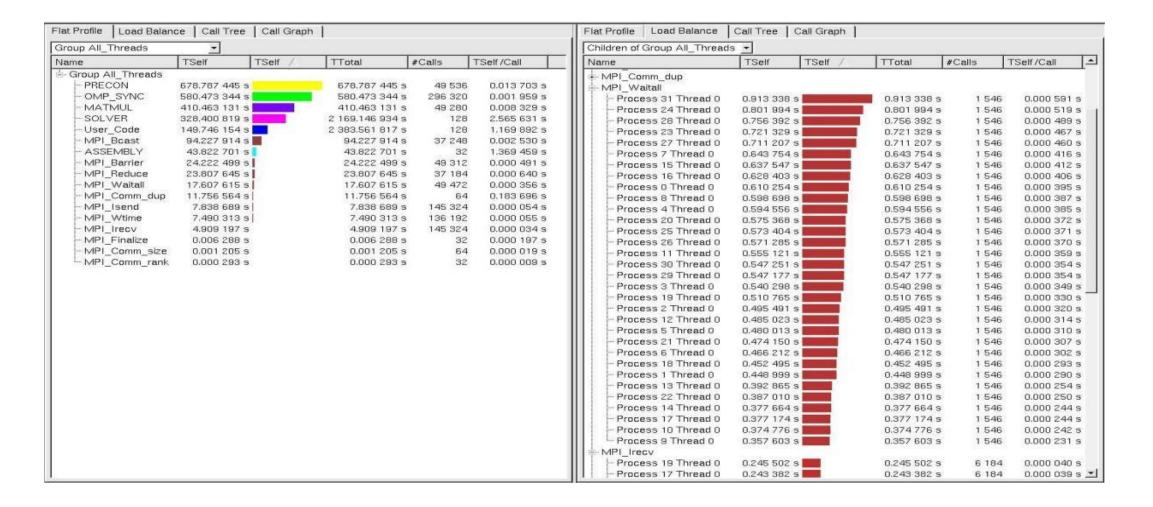
- Get impression on parallelism and load balance.
- Show for every function how many threads/processes are currently executing it.



OMP\_SYNC MATMUL PREGON SOLVER MPI

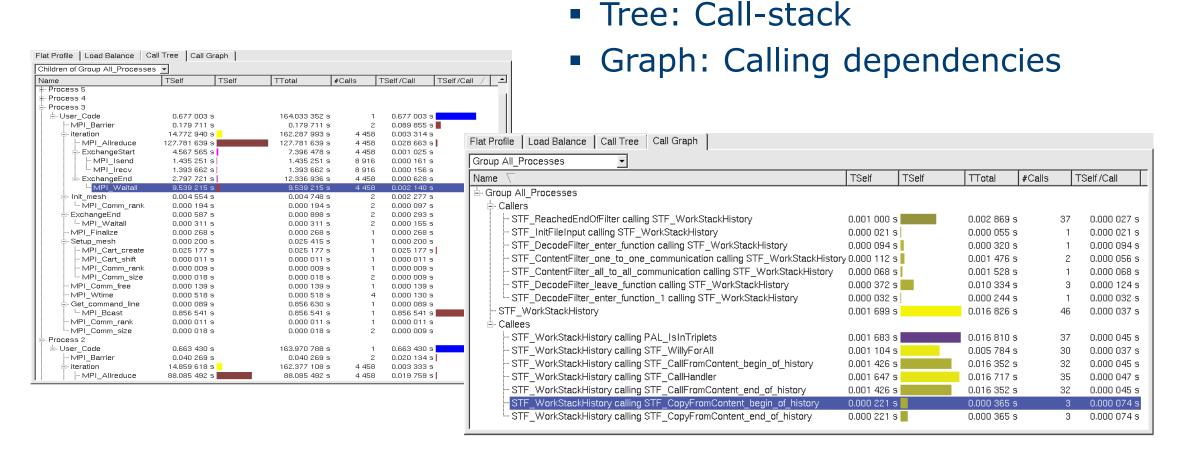
### Flat Function Profile

### **Statistics About Functions**



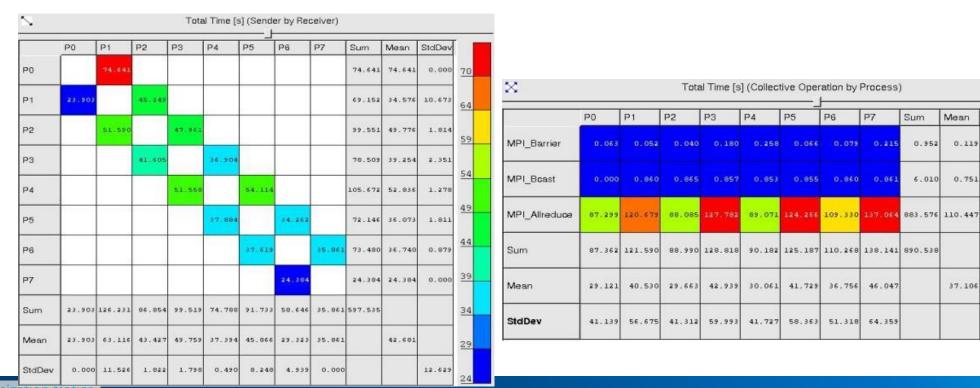
# Call-Tree and Call-Graph

### Function Statistics Including Calling Hierarchy



### **Communication Profiles**

- Statistics about point-to-point or collective communication
- Generic matrix supports grouping by several attributes in each dimension: Sender, receiver, data volume per message, tag, communicator, type
- Available attributes: Count, bytes transferred, time, transfer rate



StdDev

52.97

# BACKUP

### Platform Profiler

Collect and manage data from multiple targets easily

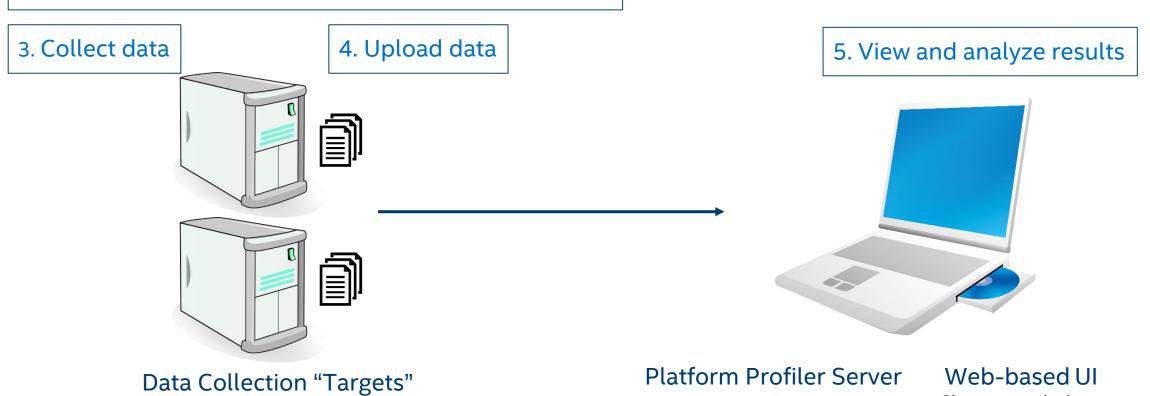
Data Collector Platform Profiler Server Web-based user interface Platform Profiler Server Web-based UI Data Collection "Targets" Chrome works best

### Workflow overview

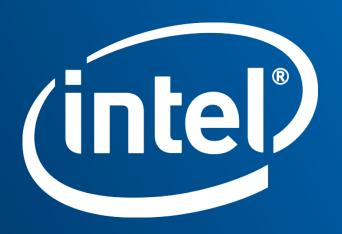
1. Install VTune and launch the Platform Profiler Server

2. Install data collector on "targets" (Linux or Windows)

Ivy Bridge or Later



Chrome works best



# Legal Disclaimer & Optimization Notice

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit <a href="https://www.intel.com/benchmarks">www.intel.com/benchmarks</a>.

INFORMATION IN THIS DOCUMENT IS PROVIDED "AS IS". NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO THIS INFORMATION INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

Copyright © 2018, Intel Corporation. All rights reserved. Intel, Pentium, Xeon, Xeon Phi, Core, VTune, Cilk, and the Intel logo are trademarks of Intel Corporation in the U.S. and other countries.

#### **Optimization Notice**

Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice.

Notice revision #20110804